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September 1983
Revised December 1999

MM74HC08

Quad 2-Input AND Gate

General Description

The MM74HC08 AND gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. The HC08 has buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

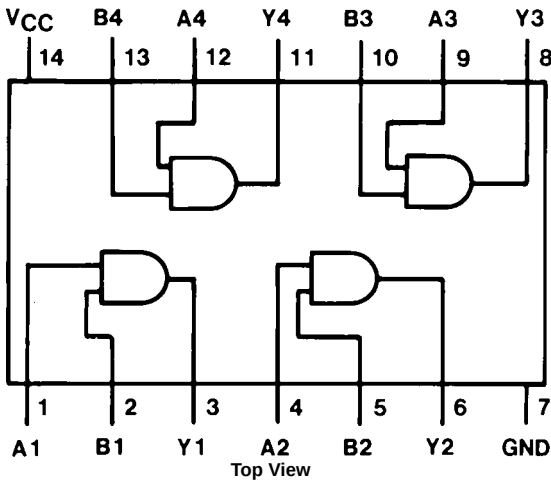
- Typical propagation delay: 7 ns (t_{PHL}), 12 ns (t_{PLH})
- Fanout of 10 LS-TTL loads
- Quiescent power consumption: 2 μ A maximum at room temperature
- Low input current: 1 μ A maximum

Ordering Code:

Order Number	Package Number	Package Description
MM74HC08M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Wide
MM74HC08SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC08MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC08N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code. (Tape and Reel not available in N14A)

Connection Diagram



MM74HC08 Quad 2-Input AND Gate

Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input Voltage (V_{IN})	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	-40	+85	°C
Input Rise or Fall Times (t_r, t_f)			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = −40 to 85°C	T _A = −40 to 125°C	Units
				Typ	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V _{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IH} I _{OUT} ≤ 20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V _{IN} = V _{IH} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
V _{OL}	Maximum LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 4: For a power supply of $5V \pm 10\%$ the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics
 $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15\text{ pF}$, $t_r = t_f = 6\text{ ns}$

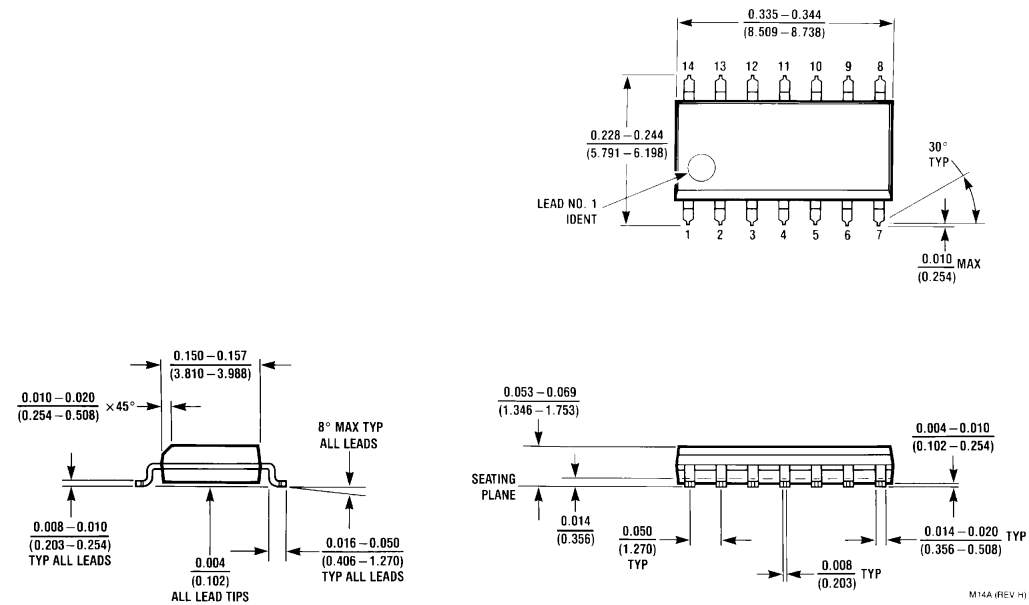
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay, Output HIGH-to-LOW		12	20	ns
t_{PLH}	Maximum Propagation Delay, Output LOW-to-HIGH		7	15	ns

AC Electrical Characteristics
 $V_{CC} = 2.0V\text{ to }6.0V$, $C_L = 50\text{ pF}$, $t_r = t_f = 6\text{ ns}$ (unless otherwise specified)

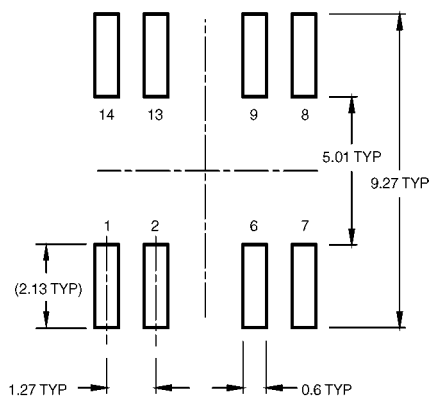
Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = −40 to 125°C	Units
				Typ	Guaranteed Limits		
t _{PHL}	Maximum Propagation Delay, Output HIGH-to-LOW		2.0V	77	121	175	ns
			4.5V	15	24	35	ns
			6.0V	13	20	30	ns
t _{PLH}	Maximum Propagation Delay, Output LOW-to-HIGH		2.0V	30	90	134	ns
			4.5V	10	18	27	ns
			6.0V	8	15	23	ns
t _{TLH} , t _{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	110	ns
			4.5V	8	15	22	ns
			6.0V	7	13	19	ns
C _{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		38			pF
C _{IN}	Maximum Input Capacitance			4	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

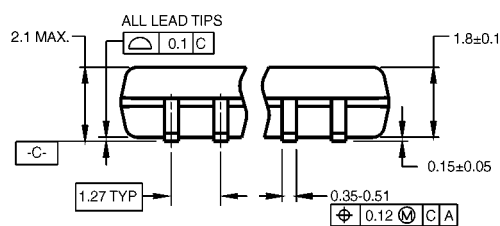
Physical Dimensions inches (millimeters) unless otherwise noted



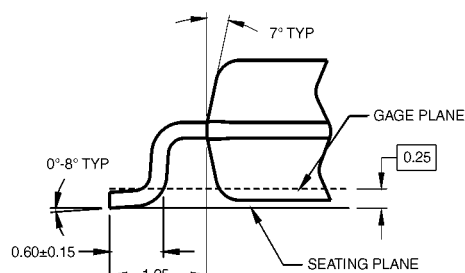
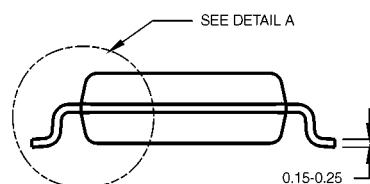
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
Package Number M14A



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

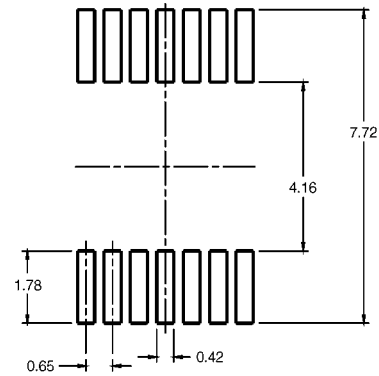
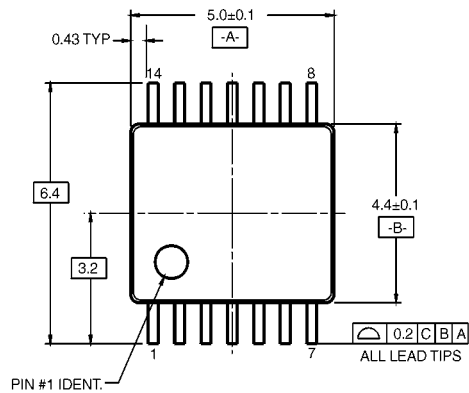
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

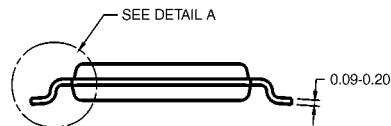
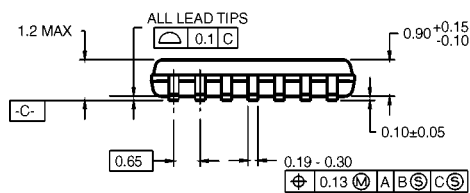
M14DRevB1

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



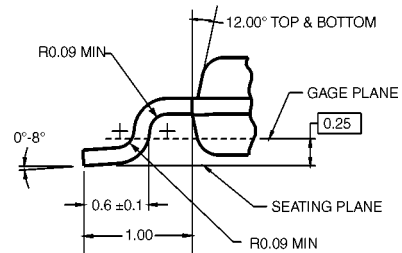
LAND PATTERN RECOMMENDATION



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

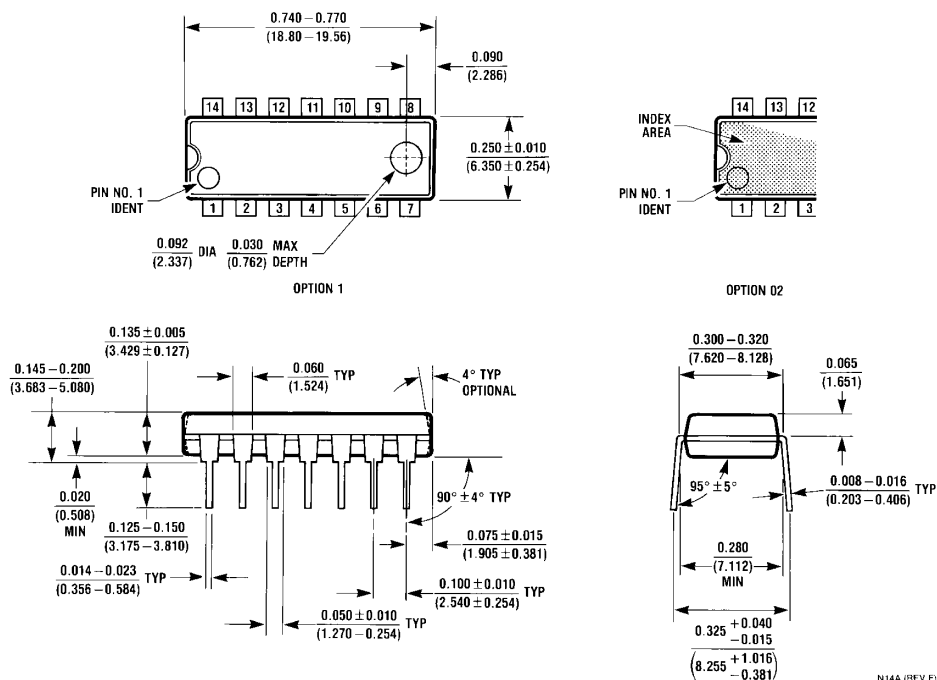
MTC14RevC3



DETAIL A

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N14A (REV F)

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